Development of CM(X Active Pixel 1 mage Sensors for Low Cost Commercial Applications

1 E.R.Fossum, R.Gee, S.E.Kemeny, Q.Kim, S.K.Mendis, J.Nakamura, R.Nixon, M.Ortiz, 11.1'sin, Z.Zhou
Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California 91109 USA
B.D.Ackland, A.Dickinson, E-S.Eid, and D.Inglis
A T&T Bell Laboratories, Holmdel, New Jersey 07733 *USA*

Abstract

This paper describes on-going research and development of CMOS active pixel image sensors for low cost commercial applications. A number of sensor designs have been fabricated and tested in both p-well and n-well technologies. Major elements in the development of the sensor include on-chip analog signal processing circuits for the reduction of fixed pattern noise, on-chip timing and control circuits and on-chip analog-to-digital conversion (ADC). Recent results and continuing efforts in these areas will bc presented.

introduction

Charge-coupkd devices (CCDs) have achieved a status of technology-of-ch oice for most imaging applications and have achieved an i mpressive level of performance. CCDs can bc fabricated in television formats (e.g. 640x480) with on-chip color lenses for less than $20 per chip for vertically integrated industries. Unfortunately, such chips arc not readily available to the low-volume user and usc of a "CCD foundry" can dramatically increase per-chip costs. Fabrication of a CCD Wafer lot in a 4-inch line is about the same cost as a CMOS wafer lot in a 6-inch line, with about 1/3 the usable wafer area. '1'bus, for many users, a CMOS image sensor technology could reduce image sensor costs by as much as 300%. Furthermore, CCDS duc to their intrinsically large capacitances, arc not readily amenable to integration of on-chip timing, control and drive electronics. Conventional CMOS signal processing circuitry is unavailable on-chip without incurring significant additional cost. Thus, these functions must bc performed off-chip by separate ICs. Hence, system integration costs of power supplies, timing and control ICs, drive electronics, signal processing ICs, and analog-to-digital converter ICs can far outweigh the advantages of a capt ive low-cost CCD fab Ii nc, even if onc were available.

This paper describes the development of a CMOS image sensor utilizing active transistors within each pixel to buffer the photosignal and provide increased sensitivity and noise rejection. This so-called active pixel sensor approach [1], while still in its infancy, has already produced reasonable quality images using conventional CMOS technology [2].

Technology Development Roadmap

The thematic goal of our activities is to develop a "camera-on-a-chip" that has a full digital interface. Only digital signals and power arc input to the chip, and only digital data is transmitted off chip. '1'here arc four major VLSI thrusts in the development activity. These arc (1) development of on-chip timing and control circuitry, (2) development of a high performance image sensor pixel for deployment in an array configuration, (3) development of colunm-wise analog circuits for noise rejection, and (4) development of low-power on-chip ADC circuits.

A. On-Chip Timing and Control Circuitry

This circuit development activity can bc considered the most straight forward part of the overall effort. in the 128x128 CMOS APS device reported in ref. [2], two 7-input NAND decoders were used for row and column selection with external circuits used to step through all possible addresses and "raster-scan" the output of the sensor. such x-Y addressability is desired for several scientific and machine vision applications to scan multiple small windows and to sub-sample images, but is not typically required for image acquisition for computers or other consumer products. Thus on-chip scanning is desired. Readout rate, integration time, and windowing functions arc to bc downloaded to the chip as part of mode control in an initial set-up phase of chip operation. Once set, the chip operates in the commanded mode until further programming is received. The first implementation of these functions is presently being completed for fabrication in 1,2 micron, single poly, double metal CMOS with 20 micron pixel pitch.

B. Pixel Development

The basic pixel structure used in the previously reported CMOS APS imager is shown below in Fig. 1. The main approach is to utilize intra-pixel charge transfer to enable correlated double sampling (CDS) type of operations. Briefly,

charge is integrated under the photogate (PG). Pixels arc selected a row al a time, using the selection switch S. The floating diffusion (FD) is reset by pulsing the reset transistor (R), and then the source-foliowcr is read out onto a sample and hold capacitor (Cr) located at the bottom of each column. The photosignal accumulated under PG is then transferred to the floating diffusion and the ncw source-follower output is stored on the other sample and hold capacitor (Cs). Columns arc selected and the voltage on both capacitors is read out as a differential pair of signals off chip. This approach removes kTC noise through CDS, as well as fired pattern noise (FPN) duc to pixel transistor offsets, and 1/f noise. It int roduces additional kTC noise duc to the sample and hold capacitors and FPN duc to unmatched column source-follower transistors,

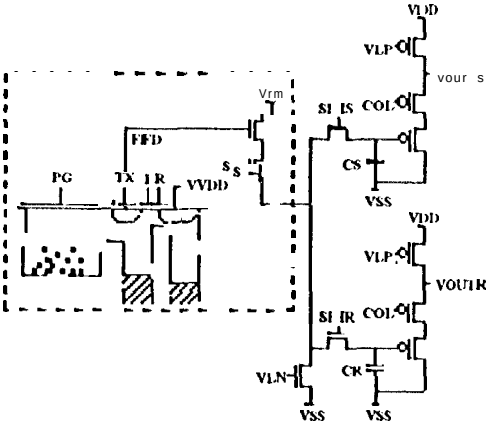

Fig. 1. Basic APS pixel circuit, Circuit located outside of dotted line is located at bottom and common to all pixels in column,

Several different layouts of the same circuit have been designed and tested in order to optimize either optical aperture (a.k.a. fill-factor or active area) or to form a more regular active area (e.g. square to simplify future integration with on-chip microlenses) vs. an irregular shape. A laser spot scanner has been used to probe the intra-pixel response for different layout configurate ions and both n-well and p-well configurat ions. For example, the n-well device was found to have much higher optical response with somewhat higher inter-pi~c] crosstalk, yet also exhibited higher dark current.

in addition to the floating diffusion approach illustrated in Fig. 1, wc have also explored floating gate readout for non-destructive sampling. In addition, non-overlapping single poly designs with inter-gale floating diffusion have been examined to better understand noise and lag issues associated with such a structure. Single poly designs arc more compatible with sub-micron CMOS fabrication lines. Wc have also looked at simple photodiode arrays buffered by the in-pixel source-follower. While suffering from higher noise, they offer higher optical response leading to an interesting trade. Some of these pixel issues will be reported in ref. [3].

C. Noise Rejection Circuits

Duc to mismatches in the column-wise Source-follower circuits, FPN levels of approximately 3.3% of saturation persist in the first generation of CMOS APS devices. Temporal noise is typically 20-40 c- rms. More advanced approaches for reducing temporal and fixed pattern noise arc being explored. The usc of a simple gain stage and ac-coupled clamp circuit to boost signal and reduce kTC noise has been designed and is presently being fabricated. Simple op-amp circuits with auto-zeroing to remove FPN arc also being simulated for future implementation. Removal of FPN is critical to the future success of the CMOS APS.

D. On-Chip A/D Converter

Wc have found the trade space for lower resolution (8-bit) ADC architectures to bc somewhat flat so that several approaches for on-chip A/D conversion arc being concurrently explored. A colunm-parallel approach is being used to reduce bandwidth and total IC power requirements. An imager with column-parallel single-slope ADCs for 8-bit resolution has been fabricated and is currently under test. A first order Σ–Δ ADC with a simple counter for the digital filter has been tested, A second order Σ–Δ ADC has been designed and fabricated for higher resolution applications.

Summary Discussion

The NASA R&D of highly integrated imaging systems for miniaturized deep space instruments has led us to explore possible commercial applications of this technology. It is apparent that the CMOS APS approach has high potential to open new markets for low cost, non-camcoder Consumer imaging systems. As the technology improves, higher performance sensors may displace CCDs in many applications.

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